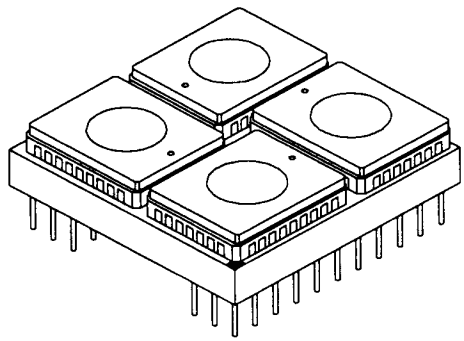
# DPV6432V

## 64K X 32 UVEPROM VERSAPAC



### DESCRIPTION:

The DPV6432V is a 66-pin Pin Grid Array (PGA) consisting of four 64K X 8 UVEPROM devices in ceramic LCC packages surface mounted on a co-fired ceramic substrate with matched thermal coefficients. The LCCs are mounted in a rotary pattern resulting in the smallest possible module outline.

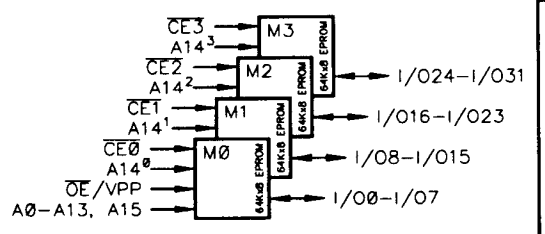
The pins have been arranged around a central 0.6" gap which can accommodate a heat rail, if desired. In this central gap is a cavity containing four 0.1µf decoupling capacitors.

### FEATURES:

- Organizations Available:
  256K X 8, 128K X 16 or 64K X 32
- Access Times:
  55*, 70, 90, 120, 150, 170, 200, 250ns
- Fully Static Operation - No clock or refresh required
- Programming Voltage 12.5 Vdc
- Simple Programming Requirements
- Three-State Outputs
- High Speed Programming Algorithm (1.0ms Pulses Typ.)
- Common Data Inputs and Outputs
- TTL-compatible Inputs and Outputs
- 66-Pin PGA (Pin Grid Array) Package
- Same Package as other Versapac Versions (EEPROM, SRAM and MIXED)
- Module Weight is 15 grams

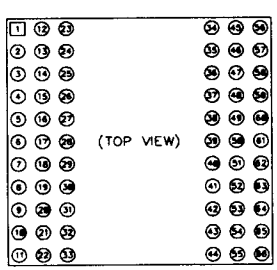
* Commercial only.

### FUNCTIONAL BLOCK DIAGRAM




| PIN NAMES | |
|---|---|
| A0-A13, $A14^0$-$A14^3$, A15 | Address Inputs |
| I/O0-I/O31 | Data In/Out |
| $\overline{CE0}$ - $\overline{CE3}$ | Chip Enables |
| $\overline{OE}$ / $V_{PP}$ | Output Enable / Programming Voltage |
| $V_{DD}$ | Power (+5V) |
| $V_{SS}$ | Ground |
| N.C. | No Connect |

### PIN-OUT DIAGRAM




| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | I/O8 | 12 | $\overline{WE1}$ | 23 | I/O14 | 34 | I/O24 | 45 | VDD | 56 | I/O3Ø |
| 2 | I/O9 | 13 | $\overline{CE1}$ | 24 | I/O13 | 35 | I/O25 | 46 | $\overline{CE3}$ | 57 | I/O29 |
| 3 | I/O1Ø | 14 | VSS | 25 | I/O12 | 36 | I/O26 | 47 | $\overline{WE3}$ | 58 | I/O28 |
| 4 | A13 | 15 | I/O15 | 26 | I/O11 | 37 | A6 | 48 | I/O31 | 59 | I/O27 |
| 5 | A15 | 16 | A1Ø | 27 | $\overline{OE}$/VPP | 38 | A7 | 49 | A3 | 6Ø | AØ |
| 6 | N.C. | 17 | A11 | 28 | N.C. | 39 | N.C. | 5Ø | A4 | 61 | A1 |
| 7 | N.C. | 18 | A12 | 29 | $\overline{WE0}$ | 4Ø | A8 | 51 | A5 | 62 | A2 |
| 8 | N.C. | 19 | VDD | 3Ø | I/O6 | 41 | A9 | 52 | $\overline{WE2}$ | 63 | I/O22 |
| 9 | I/OØ | 2Ø | $\overline{CE0}$ | 31 | I/O5 | 42 | I/O16 | 53 | $\overline{CE2}$ | 64 | I/O21 |
| 1Ø | I/O1 | 21 | N.C. | 32 | I/O4 | 43 | I/O17 | 54 | VSS | 65 | I/O2Ø |
| 11 | I/O2 | 22 | I/O7 | 33 | I/O3 | 44 | I/O18 | 55 | I/O23 | 66 | I/O19 |

FOR FURTHER INFORMATION
SEE CHAPTER 10
FOR COMPLETE DATA SHEET